IN THE UNTED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First-Named Inventor: Franciscus WIDDERSHOVEN	Atty Docket No.: **NL000722**
Application No.: 10/023,165 Conf.: 5094	Art Unit: 2188
Date Filed: 12/18/2001	Examiner: John M. ROSS
Customer No.: 24738	

Title: DATA PROCESSING DEVICE WITH WOM MEMORY

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BRIEF IN SUPPORT OF AN APPEAL

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Date: 11/14/05

Respectfully submitted,
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**WIDDERSHOVEN**
Application No.	:	**10/023,165**
Filed	:	**December 18, 2001**
For	:	**DATA PROCESSING DEVICE WITH A WOM MEMORY**

APPEAL BRIEF

On Appeal from Group Art Unit 2188

Date: November 14, 2005

By: Michael Ure
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Daniel Michalek
(Name)

(Signature and Date) 14-NOV-05.

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NONE

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-4 are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates methods and apparatus for minimizing erasures of a memory medium. As recited in claim 1, a logical series of multiple memory locations is identified and is treated in effect as a single logical memory location. A value to be stored is encoded and written initially to a first location in the series. As the value is to be

modified to a new value, the new value is encoded taking into account the current encoded value and, if feasible, stored in the current location (Specification, page 5, lines 11-16); if not feasible (i.e., because of code exhaustion), then the encoded new value is written to a next available location; or, if there is no next location available, the contents of the locations in the series are reset (Specification, page 6, lines 4-15).

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-4 are unpatentable over Rivest in view of Sinclair.

VII. ARGUMENT

I. Rejection of Claims 1-4 as Being Unpatentable over Rivest in view of Sinclair

As previously stated, the present invention relates methods and apparatus for minimizing erasures of a memory medium. As recited in claim 1, a logical series of multiple memory locations is identified and is treated in effect as a single logical memory location. A value to be stored is encoded and written initially to a first location in the series. As the value is to be modified to a new value, the new value is encoded taking into account the current encoded value and, if feasible, stored in the current location; if not feasible (i.e., because of code exhaustion), then the encoded new value is written to a next available location; or, if there is no next location available, the contents of the locations in the series are reset.

Rivest describes "reusing" or "rewriting" a non-erasable memory. Such writing and rewriting is illustrated in Fig. 1 of Rivest. Two data bits are mapped to three write-once bit positions (WITS). For example, 00 is mapped to 000, 01 is mapped to 100, etc. To write a different two bits to a previously-written location, the two data bits are mapped to the same three WITS but with a different mapping in which one need only change zeros to ones. For example, the two bits 00 are mapped to 111 and can be stored in a location that previously stored the bits 10, mapped to 101. Only the second WIT needs to be changed from zero to one. Decoding of the data is accomplished by exclusive-ORing adjacent WITS (Rivest col. 4, lines 33-39).

In Rivest, there is no identification of a logical series of multiple memory locations.

Sinclair relates to disk emulation using a FLASH memory. A algorithm is disclosed that ensures that an erased block of FLASH memory is always "at the ready," since erasure takes some time. Note, for example, col. 6, lines 63-37. Sinclair also fails to teach or suggest the logical series of multiple memory locations performing the functions set forth in claim 1.

Accordingly, claim 1 and its dependent claims are believed to patentably define over the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: November 14, 2005

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A data processing device comprising a memory having locations, each capable of storing a WOM codeword from a WOM code; a memory selector for selecting a currently selected location of a logical series of the locations; a data encoder that encodes a received data value in a new codeword from the WOM code, as a function of the received data value and a previous codeword stored in the currently selected location, the data encoder causing the currently selected location to be changed to a next one in the logical series when the WOM code is exhausted, the data encoder storing the new codeword in the currently selected location; a reset circuit for resetting a content of the locations in the logical series, the reset circuit being triggered when the WOM code is exhausted for all the locations of the logical series.

2. A data processing device according to claim 1, wherein the memory selector is arranged to determine the currently selected location from a content of the locations, so that the currently selected location has an immediate predecessor location, if any, that contains a codeword indicating that the location is full and an immediate successor location, if any, that contains an initial codeword value produced by resetting.

3. A data processing device according to claim 1, comprising an input for receiving a dataword; an error correcting encoder, arranged to form N data values, each data value at least representing a respective part of the dataword encoded in an error correcting code; the memory selector being arranged to select N currently selected locations, each of a respective logic series of the locations; the data encoder encoding the data values in N respective new codewords from the WOM code, each as a function of a respective one of the data values and a previous codeword stored in the currently selected location of a respective one of the logic series, the data encoder causing the currently selected location or locations to be changed for those of the logic series in which the WOM code is exhausted, the encoder storing each new codeword in the currently selected location of a respective one of the series; the reset circuit being triggered for those of the logic series

where WOM code is exhausted for all locations in of the logic series.

4. A data processing device according to claim 1, said series of locations being one of a plurality of logical series of locations comprised in the memory, the data processing device comprising an address input for receiving an address value corresponding to the data; a series selector for selecting, under control of the address value, the series of locations operated upon by the memory selector, the data encoder and the reset circuit.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE